31.2 A 90nm CMOS 1.2V 6b 1GS/s Two-Step Subranging ADC

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Optical and magnetic data storage front-ends and UWB communication systems require moderate resolution ADCs with high f_s that are capable of handling high-frequency input signals with a good linearity. This paper presents a 90 nm CMOS 1.2V 6b 1GS/s ADC that occupies 0.13mm^2 and consumes 55mW.

The flash architecture, usually chosen to implement high f_s ADCs, has one comparator to determine *each* code transition level [1]. This leads to high speed, but an N-bit ADC requires 2^N-1 comparators. The two-step subranging ADC on the other hand uses less hardware. A coarse flash ADC (CADC) quantizes the MSBs. The set of references closer to the input signal are then applied to a fine ADC (FADC) that quantizes the LSBs. Although this architecture uses less comparators, it is slower than the flash ADC. The utilization of two time-interleaved FADCs, as shown in Fig. 31.2.1, increases the effective sampling rate [2].

Figure 31.2.2 shows the time interleaving diagram (the operations indicated in the shaded areas will be explained later). The first sample, $v_I[1]$, is taken simultaneously by the CADC and the FADC A, at the end of $\phi1$. The CADC quantizes $v_I[1]$ during $\phi2$, so that the set of reference voltages nearer $v_I[1]$ are applied to the FADC A in $\phi3$. The comparators of the FADC A regenerate in $\phi4$, finalizing the quantization of $v_I[1]$. In $\phi3$ the CADC and the FADC B sample $v_I[2]$, and a similar quantization process occurs. The input is sampled by the CADC and one of the FADCs in every clock cycle.

Unless an offset reduction technique is used in the comparators, the large devices needed to guarantee the required resolution will lead to a high power dissipation. Offset sampling techniques introduce additional capacitors in the signal path, do not cancel the offset voltages of the latched comparators, and are limited by charge-injection mismatches in the MOS switches. The background offset calibration used in this paper overcomes these limitations.

Figure 31.2.3 depicts 1 of the 16 comparators of the FADC A (FADC B uses the same comparators, except for the timing). The input signal is sampled in a distributed way by the input capacitive networks which also subtract the sampled input from the reference voltages selected by the CADC. This is applied to a static pre-amplifier that is followed by a dynamic latched comparator. An auxiliary differential pair is added to implement the offset calibration.

The input of the pre-amplifier is shorted during $\phi1$, and its output voltage only depends on its offset. During $\phi2$ the FADC A is waiting for the CADC decision (see Fig. 31.2.2) and, thus, could be idle. Instead, the latched comparator makes a decision based on the pre-amplifier output voltage at the end of $\phi1$. The result is determined by the offset voltage of the complete comparator chain.

A simple control logic takes this result and adjusts the calibration voltage at the input of the auxiliary differential pair. This is made by pre-charging C_P to either V_{MAX} or V_{MIN}, depending on the comparator decision, and then switching C_P to C_{CAL}. As C_{CAL}>>C_P, the calibration voltage is adjusted in small steps, until the auxiliary differential pair injects a current that cancels the offset voltages of both the pre-amplifier and latched comparator. This process is always running in background, and allows using transistors smaller than 0.5µm^2, thus maximizing speed and minimizing power dissipation.

The mismatches between S_{1a}/S_{1b} cause different charge injections to the input nodes of the pre-amplifier, when they open. In usual implementations they are switched simultaneously with S_2 (S_2 does not even exist in some designs), causing an offset that is not compensated by the calibration. A large C_S makes this effect negligible, but affects the ADC operating speed and input capacitance. Instead S_{1a} and S_{1b} are switched on during $\phi4$, and the charge-injection difference is eliminated by S_2, later at $\phi1$. As there is a single S_2, no offset is produced when it opens. This allows to down-size C_S to 15fF.

In the example of Fig. 31.2.4a, V_1 to V_3 are the reference voltages of 3 comparators of the CADC (C_{C1} to C_{C3}), and the input signal is slightly below V_2. This figure shows the reference voltages provided to the FADC, for the two possible outcomes of $C_{C2,}$ since an offset voltage may lead to an incorrect decision. The input signal is correctly quantized in both cases. Since the redundancy eases the offset requirements of the CADC comparators, there is no need to calibrate them.

Figure 31.2.4a also presents the situation where the speed bottleneck of this architecture occurs. That is, when v_I is close to one of the reference voltages of the CADC, the corresponding comparator may take a long time to reach a decision due to *metastability,* while all other comparators decide quickly. An SR latch is placed after every latched comparator to store its output. If the comparator is unable to reach a decision, the previous comparison result remains stored in the SR latch.

Consider the case where C_{C2} has no offset and that it previously decided 1. Due to metastability its output may change to 0 only at the end of $\phi2$. Due to the propagation delay of the digital logic that selects the reference voltages, they change somewhere *during* $\phi3$. Until that moment the reference voltages applied to the FADC A are those corresponding to the case where C_{C2} decides 1, and v_I is close to the reference voltages received by C_{F3} and C_{F4} (C_{Fx} are the FADC comparators). After the output of C_{C2} changes to 0, the reference voltages nearer v_I are now applied to C_{F11} and C_{F12}. This transition between the two cases shown in Fig. 31.2.4a requires the input networks and pre-amplifiers of the FADCs to settle in a fraction of $\phi3$.

The proposed solution is depicted in Fig. 31.2.4b. Each FADC is split in two blocks, α and β, that have adjacent reference voltages, but whose order can be swaped. When v_I moves between adjacent CADC zones only the reference voltages in one of the blocks change. In this example the selection of the reference voltages for block α does not depend on C_{C2} - it is made by the comparators not suffering from metastability. The late decision of C_{C2} makes the reference voltages on block β to change during $\phi3$, but this is less critical since the outputs of those comparators should all be 0 or 1, and an error is overcome by the bubble correction logic. This solution also reduces the number of reference-selecting switches, since each comparator now only connects to half of the CADC zones (less parasitics, faster operation).

Figure 31.2.5 shows the INL and DNL of the ADC in the normal operation and with the calibration disabled. The improvement is evident and missing codes exist when the calibration is disabled.

Figure 31.2.6 shows the SNDR and THD as a function of f_s, for three different input frequencies. An SNDR of 33.8dB (ENOB of 5.3b) is obtained for f_s=1GHz and f_i=502MHz. Limitations in the test equipment did not allow to perform measurements at larger f_i and f_s. Figure 31.2.7 shows the chip micrograph. The FADCs are not implemented as separate converters: the corresponding comparators in the two FADCs are placed side-by-side, sharing the same local phase-buffers and input/reference voltage lines, thus minimizing interchannel mismatches.

Acknowledgment:
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References:
[1] X. Jiang et al., "A 2GS/s 6b ADC in 0.18µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 322-323, Feb., 2003.
[2] A. Wiesbauer et al., "A Fully Integrated Analog Front-End Macro for Cable Modem Applications in 0.18-µm CMOS," *IEEE J. Solid-State Circuits*, vol. 37, no. 7, pp. 866-873, July, 2002.

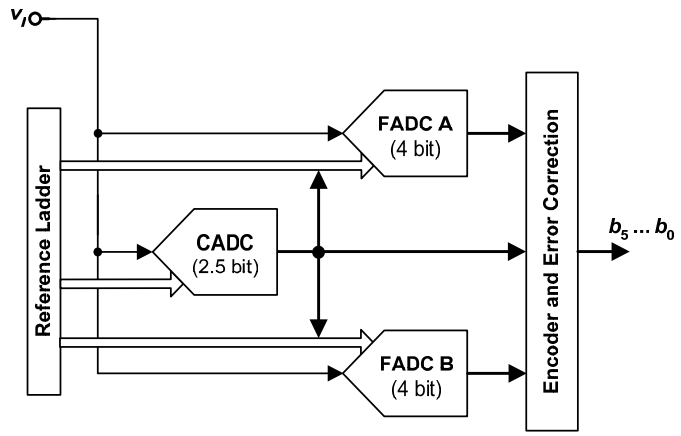

Figure 31.2.1: 6b two-step subranging architecture.

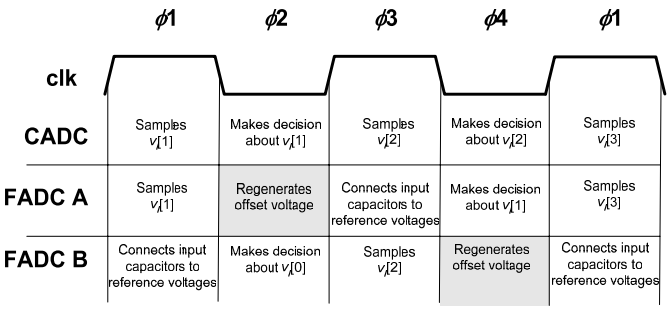

Figure 31.2.2: Timing diagram.

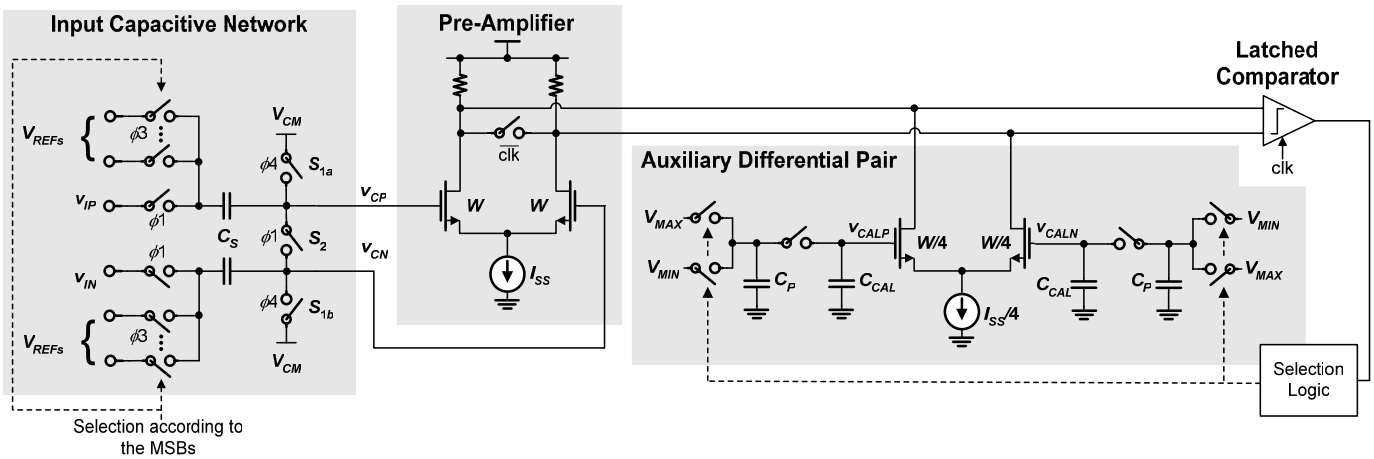

Figure 31.2.3: FADC A comparator.

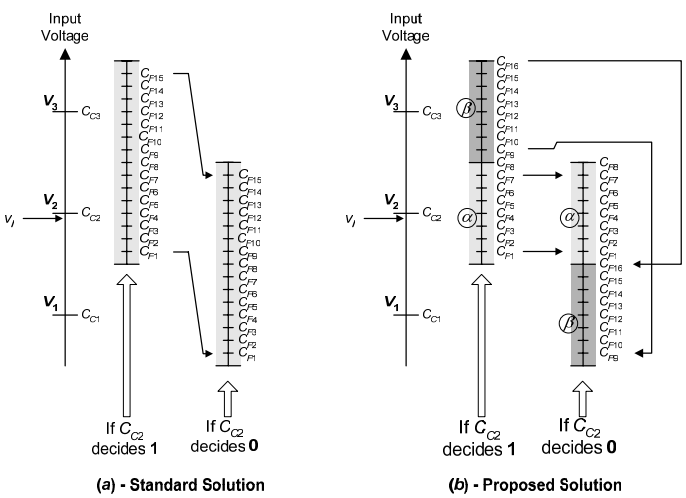

Figure 31.2.4: Reference voltages provided to the FADCs.

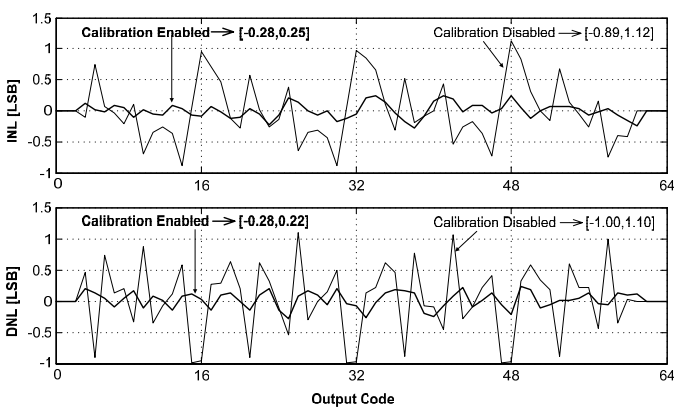

Figure 31.2.5: Typical INL and DNL.

Continued on Page 673

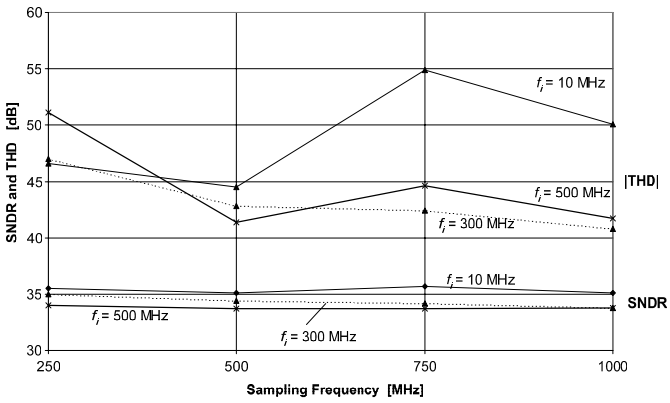

Figure 31.2.6: THD and SNDR as a function of f_s, for 3 different f_i.

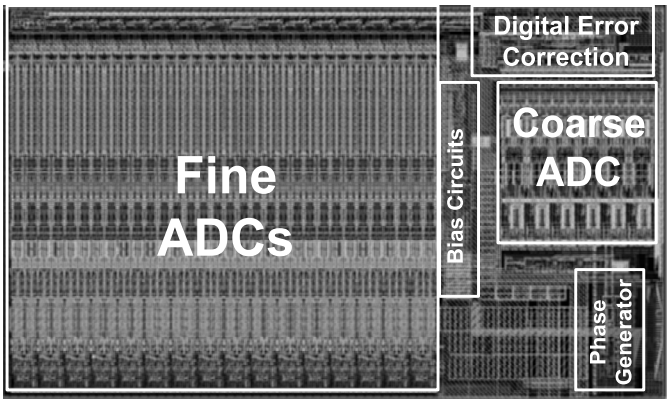

Figure 31.2.7: Chip micrograph.

